Abstract of the Disclosure

An MOS device comprises a semiconductor layer of a first conductivity type and first and second source/drain regions of a second conductivity type formed in the semiconductor layer proximate an upper surface of the semiconductor layer. The first and second source/drain regions are spaced laterally apart relative to one another and are formed in an active region of the semiconductor layer. The MOS device further comprises a gate formed above the semiconductor layer proximate the upper surface of the semiconductor layer and at least partially between the first and second source/drain regions. The gate is configured such that a dimension of the gate, defined substantially parallel to at least one of the first and second source/drain regions, is confined to be substantially within the active region of the device. An isolation structure is formed in the semiconductor layer, the isolation structure being configured to substantially isolate the first source/drain region from the second source/drain region.